PAT-NO: JP405218431A

DOCUMENT-IDENTIFIER: JP 05218431 A

TITLE: FIELD EFFECT TRANSISTOR

PUBN-DATE: August 27, 1993

INVENTOR-INFORMATION:
NAME
FUNAKI, MASANORI

ASSIGNEE-INFORMATION:
NAME COUNTRY
VICTOR CO OF JAPAN LTD N/A

APPL-NO: JP04046015

APPL-DATE: January 31, 1992

INT-CL (IPC): H01L029/784, H01L027/12

ABSTRACT:

PURPOSE: To provide the title field effect transistor having high reliability without breaking down a gate oxide film.

CONSTITUTION: Within the title field effect transistor, a source region 2 and a drain region 3 implanted with impurities are formed on an insulating layer 1; a channel region 4 containing almost no impurities at all is formed between these regions 2 and 3; and then a gate region 6 is provided on the channel region 4 through the intermediary of a gate insulating film 5 comprising SiO<SB>2</SB>, etc. In such a constitution, the thickness of the source region 2 and the drain region 3 is to be thinner than that of the channel region 4 so that the surface of the source region 2 and the drain region 3 may be located on a position lower than that of the channel region 4.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to SOIMOSFET (Silicon On Insulator Metal Oxide Semiconductor Field Effect Transistor).
[0002]
[Description of the Prior Art] In the possibility of a latch rise free-lancer, soft error resistance, low stray capacity, and three-dimensions-izing of an integrated circuit etc., SOIMOSFET which has the advantage which is not in a bulk Si element attracts attention. It makes between these source field 12 and the drain fields 13 the channel field 14, and has structure which formed the gate field 16 through the oxide film 15 on this channel field 14 while this SOIMOSFET forms the silicon layer 11 on the insulator 10 of SiO2 grade, injects an impurity into a part of this silicon layer 11 and forms the source field 12 and the drain field 13, as shown in drawing 8 .
[0003] And since above SOIMOSFET can make zero most impurities of channel field 14 field unlike the usual MOSFET, it can suppress dispersion of an impurity and can make a high-speed device. By forming a thin SOI film especially, the kink effect and a drain current overshoot phenomenon can be suppressed, and highly efficient-ization can be attained.
[0004]
[Problem(s) to be Solved by the Invention] By the way, when current flows towards the drain field 13 through the channel field 14 from the source field 12 as shown in drawing 9 if it is in above-mentioned SOIMOSFET, by high electric field, the electron (hot electron) which changed into the high-energy state collides with a silicon crystal lattice, an electron and a hole pair are generated, this jumps into the gate oxide film 15, a film is destroyed, or interface level is generated, a device property is out of order, and reliability falls. Since the electric field near the drain become large when a thin SOI film is formed, especially the above-mentioned disadvantage becomes remarkable.
[0005]
[Means for Solving the Problem] That the above-mentioned technical problem should be solved, this invention formed the silicon (Si) layer on the insulator, and made thickness of the aforementioned drain field thinner than the thickness of a channel field in the field-effect transistor which injected the impurity into this silicon layer and formed the source field and the drain field.
[0006]
[Function] Since the thickness of a drain field is thinner than the thickness of a channel field, the upper surface of a drain field is located below the inferior surface of tongue of a gate oxide film, and since the path of current goes into a drain field through the portion which is separated from a strong electric-field portion as a result, the hot electron to generate can be reduced.
[0007]
[Example] The example of this invention is explained based on an accompanying drawing below. Here, the cross section of the field-effect transistor which drawing 1 requires for this invention, and drawing 2 are drawings in which the important section expanded sectional view, drawing 3 , or drawing 7 of this field-effect transistor shows the manufacture method of a field-effect transistor.
[0008] The field-effect transistor of this invention forms the source field 2 and the drain field 3 which come to pour an impurity into silicon (Si) on the insulating layer 1 of SiO2 grade, makes between these source field 2 and the drain field 3 the channel field 4 where an impurity is hardly contained, and has structure which formed the gate field 6 through the gate oxide film 5 of SiO2 grade on this channel field 4.
[0009] And the thickness is made thinner than the thickness of the channel field 4, and the aforementioned source field 2 and the drain field 3 are located in the position where the upper surface of the source field 2 and the drain field 3 fell rather than the upper surface of the channel field 4.
[0010] If voltage is impressed above to the gate field 6, resistance of the channel field 4 is controlled and current is passed between the source field 2 and the drain field 3, as shown in the arrow of drawing 2 , current will flow from the source field 2 to the drain field 3 through the channel field 4. And since the upper surface of the drain field 3 is located in the position which fell rather than the channel field 4 upper surface at this time, current avoids the portion of the highest electric field and flows into the drain field 4.

[0011] Next, the manufacture method of the above-mentioned field-effect transistor (SOIMOSFET) is explained based on drawing 3 or drawing 7 . As first shown in drawing 3 , the silicon (Si) layer 7 is formed to the thickness of about 500A by the epitaxial grown method etc. on the insulating layer 1 of SiO2 grade. Oxide-film 5a of SiO2 grade is formed in this silicon layer 7 front face, polysilicon contest layer 6a used as the gate field 6 is further formed in the front face of this oxide-film 5a, the resist mask 8 is covered over the front face of this polysilicon contest layer 6a, and it etches with the upper shell plasma of the resist mask 8 etc.

[0012] Then, if leave the portion of the resist mask 8, polysilicon contest layer 6a is removed, the gate field 6 is formed and etching is further continued as shown in drawing 4 , as shown in drawing 5 , it will leave the portion of the resist mask 8, oxide-film 5a will be removed, and the gate oxide film 5 will be formed.

[0013] Although etching will be stopped in an above position if it is the former, if it is in this invention, the silicon layer 7 further exposed from the resist mask 8 downward from the inferior surface of tongue of the gate oxide film 5 as etching is continued further and it is shown in drawing 6 is investigated.

[0014] Then, as shown in drawing 7 , impurities, such as As, can be injected into the silicon layer 7 exposed from the resist mask 8, the source field 2 and the drain field 3 can be formed, and the field-effect transistor shown in drawing 1 can be obtained by removing the resist mask 8 by ashing further.

[0015] In addition, although it was made for the thickness of a source field to also become equal to a drain field in consideration of the symmetric property of a device if it was in the example, you may make it become flat-tapped with the channel field upper surface as usual about a source field.

[0016]

[Effect of the Invention] since thickness of a drain field (Tb) is made thinner than the thickness of a channel field (Ta) and it was made for the drain field upper surface to be located below a gate oxide-film inferior surface of tongue when it was alike and was based on the SOIMOS field-effect transistor of this invention, as explained above, it can go into a drain field through the portion into which the path of current separated from the strong electric-field portion, and the hot electron to generate can be reduced Therefore, even if it makes a SOI film thin to about 500A, a gate oxide film cannot be destroyed and a reliable field-effect transistor can be obtained.

[Translation done.]

$T_b / T_a < 1$

[0011] Next, the manufacture method of the above-mentioned field-effect transistor (SOIMOSFET) is explained based on drawing 3 or drawing 7 . As first shown in drawing 3 , the silicon (Si) layer 7 is formed to the thickness of about 500A by the epitaxial grown method etc. on the insulating layer 1 of SiO2 grade. Oxide-film 5a of SiO2 grade is formed in this silicon layer 7 front face, polysilicon contest layer 6a used as the gate field 6 is further formed in the front face of this oxide-film 5a, the resist mask 8 is covered over the front face of this polysilicon contest layer 6a, and it etches with the upper shell plasma of the resist mask 8 etc.

[0012] Then, if leave the portion of the resist mask 8, polysilicon contest layer 6a is removed, the gate field 6 is formed and etching is further continued as shown in drawing 4 , as shown in drawing 5 , it will leave the portion of the resist mask 8, oxide-film 5a will be removed, and the gate oxide film 5 will be formed.

[0013] Although etching will be stopped in an above position if it is the former, if it is in this invention, the silicon layer 7 further exposed from the resist mask 8 downward from the inferior surface of tongue of the gate oxide film 5 as etching is continued further and it is shown in drawing 6 is investigated.

[0014] Then, as shown in drawing 7 , impurities, such as As, can be injected into the silicon layer 7 exposed from the resist mask 8, the source field 2 and the drain field 3 can be formed, and the field-effect transistor shown in drawing 1 can be obtained by removing the resist mask 8 by ashing further.

[0015] In addition, although it was made for the thickness of a source field to also become equal to a drain field in consideration of the symmetric property of a device if it was in the example, you may make it become flat-tapped with the channel field upper surface as usual about a source field.

[0016]

[Effect of the Invention] since thickness of a drain field (T_b) is made thinner than the thickness of a channel field (T_a) and it was made for the drain field upper surface to be located below a gate oxide-film inferior surface of tongue when it was alike and was based on the SOIMOS field-effect transistor of this invention, as explained above, it can go into a drain field through the portion into which the path of current separated from the strong electric-field portion, and the hot electron to generate can be reduced Therefore, even if it makes a SOI film thin to about 500A, a gate oxide film cannot be destroyed and a reliable field-effect transistor can be obtained.

[Translation done.]

$T_b / T_a < 1$

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The cross section of the field-effect transistor concerning this invention
[Drawing 2] The important section expanded sectional view of this field-effect transistor
[Drawing 3] Drawing showing the manufacture method of the field-effect transistor concerning this invention
[Drawing 4] Drawing showing the manufacture method of the field-effect transistor concerning this invention
[Drawing 5] Drawing showing the manufacture method of the field-effect transistor concerning this invention
[Drawing 6] Drawing showing the manufacture method of the field-effect transistor concerning this invention
[Drawing 7] Drawing showing the manufacture method of the field-effect transistor concerning this invention
[Drawing 8] The cross section of the conventional field-effect transistor
[Drawing 9] The important section expanded sectional view of the conventional field-effect transistor
[Description of Notations]
1 [-- A drain field, 4 / -- A channel field, 5 / -- A gate oxide film, 6 / -- A gate field, 7 / -- A silicon layer, 8 / -- Resist mask.]
-- An insulating layer, 2 -- A source field, 3

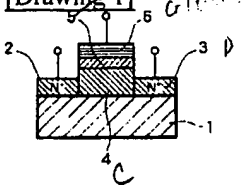
[Translation done.]

* NOTICES *

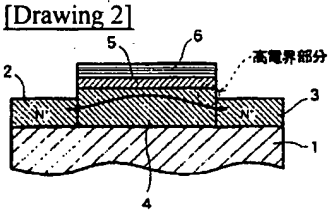
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

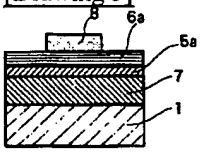
[Drawing 1]



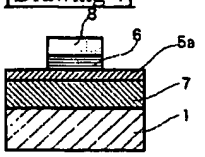
[Drawing 2]



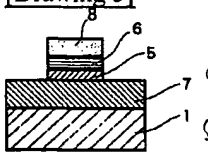
[Drawing 3]



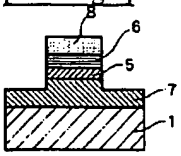
[Drawing 4]



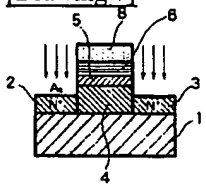
[Drawing 5]



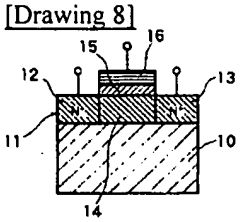
[Drawing 6]



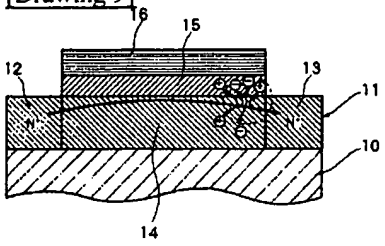
[Drawing 7]



[Drawing 8]



[Drawing 9]



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平5－218431

(43)公開日　平成５年(1993)８月27日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　29/784				
27/12		Ｚ　8728－4Ｍ		
		9056－4Ｍ	Ｈ０１Ｌ　29/ 78　　３１１　Ｓ	

審査請求　未請求　請求項の数１(全　３　頁)

(21)出願番号　特願平4－46015

(22)出願日　平成４年(1992)１月31日

(71)出願人　000004329
日本ビクター株式会社
神奈川県横浜市神奈川区守屋町３丁目12番地

(72)発明者　舟木　正紀
神奈川県横浜市神奈川区守屋町３丁目12番地　日本ビクター株式会社内

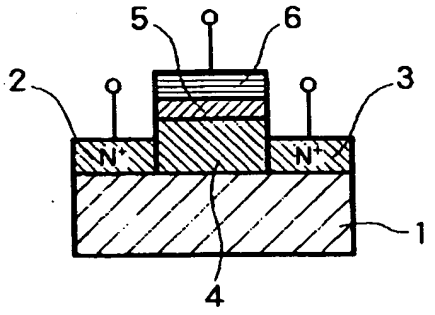
(74)代理人　弁理士　下田　容一郎　(外１名)

(54)【発明の名称】　電界効果トランジスタ

(57)【要約】

【目的】　ゲート酸化膜を破壊することがなく、信頼性の高い電界効果トランジスタを提供すること。

【構成】　絶縁層１上にシリコン（Ｓｉ）に不純物を注入してなるソース領域２とドレイン領域３を形成し、これらソース領域２とドレイン領域３間を不純物が殆ど含まれないチャネル領域４とし、このチャネル領域４上にSiO_2等のゲート酸化膜５を介してゲート領域６を設け、前記ソース領域２とドレイン領域３はその厚みがチャネル領域４の厚みよりも薄く、ソース領域２とドレイン領域３の上面がチャネル領域４の上面よりも下がった位置にある。



1

【特許請求の範囲】

【請求項1】　絶縁体上にシリコン（Ｓｉ）層を形成し、このシリコン層に不純物を注入してソース領域及びドレイン領域を形成した電界効果トランジスタにおいて、前記ドレイン領域の厚みをチャネル領域の厚みよりも薄くしたことを特徴とする電界効果トランジスタ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はＳＯＩＭＯＳＦＥＴ（Silicon On Insulator Metal Oxide Semiconductor Field Effect Transistor）に関する。

【０００２】

【従来の技術】ラッチアップフリー、ソフトエラー耐性、低浮遊容量、集積回路の三次元化の可能性等において、バルクＳｉ素子にない利点を有するＳＯＩＭＯＳＦＥＴが注目されている。このＳＯＩＭＯＳＦＥＴは図８に示すように、SiO_2等の絶縁体１０の上にシリコン層１１を形成し、このシリコン層１１の一部に不純物を注入してソース領域１２及びドレイン領域１３を形成するとともに、これらソース領域１２とドレイン領域１３との間をチャネル領域１４とし、このチャネル領域１４の上に酸化膜１５を介してゲート領域１６を形成した構造になっている。

【０００３】そして、上記のＳＯＩＭＯＳＦＥＴは通常のＭＯＳＦＥＴと異なり、チャネル領域１４領域の不純物を殆どゼロにすることができるので、不純物の散乱を抑えられ、高速のデバイスを作ることができる。特に薄いＳＯＩ膜を形成することにより、キンク効果及びドレイン電流オーバシュート現象を抑制でき、高性能化を達成することができる。

【０００４】

【発明が解決しようとする課題】ところで、上述のＳＯＩＭＯＳＦＥＴにあっては、図９に示すようにチャネル領域１４を介してソース領域１２からドレイン領域１３に向けて電流が流れる場合、高電界によって高エネルギ状態になったエレクトロン（ホットエレクトロン）がシリコン結晶格子に衝突して電子・ホール対を発生させ、これがゲート酸化膜１５に飛込んで膜を破壊したり、界面準位を発生してデバイス特性が狂い信頼性が低下する。特に、上記の不利は薄いＳＯＩ膜を形成した場合にドレイン近傍の電界が大きくなるので顕著になる。

【０００５】

【課題を解決するための手段】上記課題を解決すべく本発明は、絶縁体上にシリコン（Ｓｉ）層を形成し、このシリコン層に不純物を注入してソース領域及びドレイン領域を形成した電界効果トランジスタにおいて、前記ドレイン領域の厚みをチャネル領域の厚みよりも薄くした。

【０００６】

【作用】ドレイン領域の厚みがチャネル領域の厚みよりも薄くなっているので、ドレイン領域の上面がゲート酸化膜の下面よりも下に位置し、その結果電流の経路は強電界部分から離れた部分を通ってドレイン領域に入るので、発生するホットエレクトロンを低減することができる。

2

【０００７】

【実施例】以下に本発明の実施例を添付図面に基づいて説明する。ここで、図１は本発明に係る電界効果トランジスタの断面図、図２は同電界効果トランジスタの要部拡大断面図、図３乃至図７は電界効果トランジスタの製作方法を示す図である。

【０００８】本発明の電界効果トランジスタはSiO_2等の絶縁層１上にシリコン（Ｓｉ）に不純物を注入してなるソース領域２とドレイン領域３を形成し、これらソース領域２とドレイン領域３間を不純物が殆ど含まれないチャネル領域４とし、このチャネル領域４上にSiO_2等のゲート酸化膜５を介してゲート領域６を設けた構造になっている。

【０００９】そして、前記ソース領域２とドレイン領域３はその厚みがチャネル領域４の厚みよりも薄くされ、ソース領域２とドレイン領域３の上面がチャネル領域４の上面よりも下がった位置にある。

【００１０】以上において、ゲート領域６に電圧を印加してチャネル領域４の抵抗をコントロールしてソース領域２とドレイン領域３間に電流を流すと、図２の矢印に示すように電流はソース領域２からチャネル領域４を通ってドレイン領域３に流れる。そして、このときドレイン領域３の上面はチャネル領域４上面よりも下がった位置にあるので、電流は最も高い電界の部分を避けてドレイン領域４に流入する。

【００１１】次に、上記の電界効果トランジスタ（ＳＯＩＭＯＳＦＥＴ）の製作方法を図３乃至図７に基づいて説明する。先ず図３に示すように、SiO_2等の絶縁層１上にシリコン（Ｓｉ）層７をエピタキシャル成長法等によって５００Å程度の厚さまで形成し、このシリコン層７表面にSiO_2等の酸化膜５ａを形成し、更にこの酸化膜５ａの表面にゲート領域６となるポリシリコン層６ａを形成し、このポリシリコン層６ａの表面にレジストマスク８をかけ、レジストマスク８の上からプラズマ等でエッチングを行なう。

【００１２】すると、図４に示すように、レジストマスク８の部分を残してポリシリコン層６ａが除去されてゲート領域６が形成され、更にエッチングを継続すると、図５に示すようにレジストマスク８の部分を残して酸化膜５ａが除去されてゲート酸化膜５が形成される。

【００１３】従来であれば上記の位置でエッチングを停止するのであるが、本発明にあっては更にエッチングを継続して図６に示すようにゲート酸化膜５の下面より更に下までレジストマスク８から露出しているシリコン層７を掘り下げる。

3

【００１４】この後、図7に示すように、レジストマスク８から露出しているシリコン層７にAs等の不純物を注入してソース領域２及びドレイン領域３を形成し、更にアッシングによってレジストマスク８を除去することによって図１に示した電界効果トランジスタを得ることができる。

【００１５】尚、実施例にあってはデバイスの対称性を考慮して、ソース領域の厚さもドレイン領域と等しくなるようにしたが、ソース領域については従来と同様にチャネル領域上面と面一となるようにしてもよい。

【００１６】

【発明の効果】以上に説明したように本発明のＳＯＩＭＯＳ電界効果トランジスタににによれば、ドレイン領域の厚みをチャネル領域の厚みよりも薄くし、ドレイン領域上面がゲート酸化膜下面よりも下に位置するようにしたので、電流の経路が強電界部分から離れた部分を通ってドレイン領域に入ることとなり、発生するホットエレクトロンを低減することができる。したがって、ＳＯＩ膜を５００Å程度まで薄くしてもゲート酸化膜を破壊することがなく、信頼性の高い電界効果トランジスタを得

4

ることができる。

【図面の簡単な説明】

【図１】本発明に係る電界効果トランジスタの断面図

【図２】同電界効果トランジスタの要部拡大断面図

【図３】本発明に係る電界効果トランジスタの製作方法を示す図

【図４】本発明に係る電界効果トランジスタの製作方法を示す図

【図５】本発明に係る電界効果トランジスタの製作方法を示す図

【図６】本発明に係る電界効果トランジスタの製作方法を示す図

【図７】本発明に係る電界効果トランジスタの製作方法を示す図

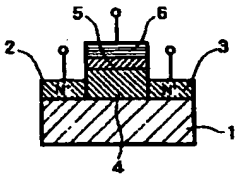
【図８】従来の電界効果トランジスタの断面図

【図９】従来の電界効果トランジスタの要部拡大断面図

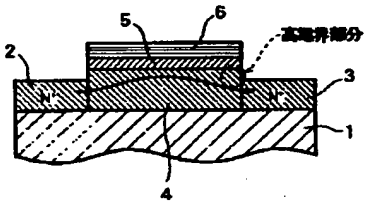
【符号の説明】

1…絶縁層、2…ソース領域、3…ドレイン領域、4…チャネル領域、5…ゲート酸化膜、6…ゲート領域、7…シリコン層、8…レジストマスク。

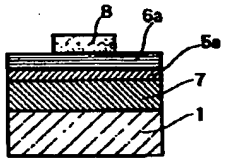
【図1】



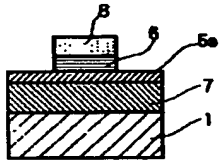
【図2】



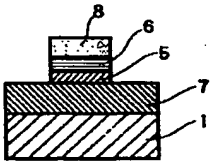
【図3】



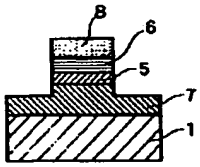
【図4】



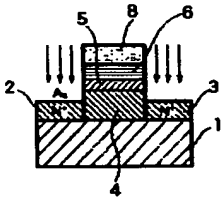
【図5】



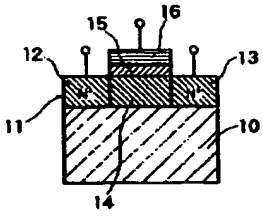
【図6】



【図7】



【図8】



【図9】